



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Patent and Trademark Administration
Washington, D.C. 20503
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAME OF INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|------------------------|----------------------------|------------------|
| 09/736,043 | 12/12/2000 | Yue Kuo | 017575-0414/1AMUS 15291 | 7225 |

7541 03/24/2003

Baker Botts L.L.P.
2001 Ross Avenue
Dallas, TX 75201-2980

EXAMINER

COLEMAN, WILLIAM D

ART UNIT PAPER NUMBER

2823

DATE MAILED: 03/24/2003

Please find below and or attached an Office communication concerning this application or proceeding.

09/736,043

KUO, YUE

Office Action Summary

Examiner

Art Unit

W David Coleman

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED, 35 U.S.C. § 133.
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 January 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 12 6) ☐ Other

DETAILED ACTION

Response to Arguments

1. The amendment filed January 9, 2003 in paper no. 10 is not persuasive.
2. Applicants contend that the art rejection of Gardner et al., U.S. Patent 5,350,484 in view of Allen, et al., U.S. Patent 5,736,002 pertaining to claims 1-5 and 7-30 fail to teach Applicants invention because the cited art fails to show a "plasma deposition reactor" or use the term "plasma deposition reactor".
3. In response to Applicants argument that the combined art of Gardner in view of Allen fail to show or use the term "plasma deposition reactor", please note that Gardner discloses more than one embodiment and it is highly suggested that Gardner substantially teaches Applicants claimed invention. Applicants may not be familiar with deposition processes or the plasma physics required to form a plasma. However, Gardner teaches i.e., *"In the fabrication of metal interconnects according to the present invention, as shown in FIG. 1, a metal film is deposited on a silicon layer 14 of a substrate 1 during the fabrication of a semiconductor device by techniques well-known in the art, such as CVD, sputter deposition (emphasis added)"* [column 3, lines 63-68]. Furthermore Gardner teaches a conversion step by driving ions 9 into the exposed region 6 of the metal film 3 by techniques well-known in the art which includes ion implantation (column 4, lines 21-26). Ion implantation is a plasma deposition process and it is well known to require a reactor (vacuum chamber) to perform such a process and therefore would suggest Applicants claimed invention.
4. With regards to Applicants traversal of claims 31 and 32 and in particularly the use of a plasma etcher please note the following. The major difference between plasma deposition and

plasma etching is highly dependent on where a biased voltage is applied in the system. Please note that when one is using a plasma etcher a bias is applied to the work piece and deposition is occurring on the walls of the chamber. When the walls of the chamber need to be cleaned, a bias is applied to the chamber walls and the vacuum through put is used to allow the deposits to be removed from the chamber.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-4, 7-11, 13-20 and 22-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al., U.S. Patent 5,350,484 in view of Allen et al., U.S. Patent 5,736,002.

7. Pertaining to claims 1, 11 and 18, Gardner discloses a semiconductor process substantially as claimed. See **FIGS. 2A-2C**, where Gardner teaches a method for forming a conductive pattern for a semiconductor device comprising:

patterning a mask layer **4** outwardly from a conductive layer **3** of the semiconductor device, the patterning defining portions **6** of the conductive layer **3** where vias through the conductive layer **3** are desired;

exposing the semiconductor device to a plasma **10** using a plasma deposition reactor (please note that an ion implanter is a plasma deposition reactor), the plasma converting the unmasked portions of the conductive layer **3** into a compound **8**; and

Art Unit: 2823

exposing the semiconductor device to a treatment process, the treatment process selectively removing the compound (column 8, lines 22-27). However, Gardner fails to teach wherein exposing the semiconductor device to a treatment comprises:

exposing the semiconductor device to a substantially inert atmosphere; and

heating the semiconductor device to between 300 and 800 degrees Celsius while the semiconductor device is exposed to the substantially inert atmosphere to remove the compound.

Allen teaches wherein exposing the semiconductor device to a treatment comprises:

exposing the semiconductor device to a substantially inert atmosphere; and

heating the semiconductor device to between 300 and 800 degrees Celsius while the semiconductor device is exposed to the substantially inert atmosphere to remove the compound.

See columns 9 and 10 where Allen teaches wherein exposing the semiconductor device to a treatment comprises:

exposing the semiconductor device to a substantially inert atmosphere; and

heating the semiconductor device to between 300 and 800 degrees Celsius while the semiconductor device is exposed to the substantially inert atmosphere to remove the compound (please note that Allen teaches vaporizing copper up to 2000 degrees Celsius and therefore meets the claim limitations). In view of Allen, it would have been obvious to one of ordinary skill in the art to incorporate the process steps of Allen into the Gardner semiconductor process because in theory, copper chloride, copper fluoride and copper oxide can all be selectively removed from copper by vaporization (column 9, lines 54-58).

8. Pertaining to claims 2 and 28, Gardner teaches wherein the conductive layer 3 comprises a copper material (column 6, lines 55-56).

Art Unit: 2823

9. Pertaining to claim 3, Gardner teaches removing the mask layer **4** from the semiconductor device **1**.
10. Pertaining to claims 4 and 20, Gardner teaches removing the mask layer **4** after removing the compound **8**.
11. Pertaining to claims 7 and 15, Gardner teaches providing a barrier layer **2** between the conductive material **3** and the substrate (not numbered).
12. Pertaining to claims 8 and 14, Gardner teaches wherein the conductive material **3** comprises a copper material, and wherein exposing the semiconductor device to a plasma **10** comprises exposing the semiconductor device to a chlorine-containing gas (column 7, line 26).
13. Pertaining to claims 9, 23, 24, 25, 26, 29 and 30, Gardner teaches wherein the compound comprise a copper chloride material **8**, and wherein exposing the semiconductor device to a treatment process comprises exposing the semiconductor device to a hydrogen chloride solution to remove the copper chloride material (See table III).
14. Pertaining to claims 10, 17 and 19, Gardner teaches wherein the mask layer comprises a photoresist material **5**.
15. Pertaining to claim 13, Gardner teaches wherein forming a conductive layer **3** comprises forming a copper layer outwardly from the substrate.
16. Pertaining to claims 16, 22 and 27, Gardner teaches wherein exposing the electronic device to a plasma comprises controlling the exposure of the electronic device to the plasma **10** to form a substantially perpendicular interface between the masked conductive material **3** and the compound **8**.

Art Unit: 2823

17. Claims 5, 12 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al., U.S. Patent 5,350,484 in view of Allen et al., U.S. Patent 5,736,002 as applied to claims 1-4, 7-11, 13-20 and 22-30 above.

18. Gardner teaches a semiconductor process substantially as claimed, however, Gardner fails to teach the selection of removing the masking layers before removing the compound. Applicant is reminded that selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results. In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946). However, in the absence of new or unexpected results, the mere reversal of the order of performing process steps has been held to be prima facie obvious. In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

Claim Rejections - 35 USC § 102

19. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

20. Claims 31 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Allen et al., U.S. Patent 5,736,002.

21. Pertaining to claim 31, see **FIGS. 2, 3 and 4A**, where Allen discloses a method for forming a conductive pattern for a device, comprising:

patterning a mask layer **240** outwardly from a conductive layer **420** of the device, the patterning defining portions of the conductive layer where vias through the conductive layer are desired;

Art Unit: 2823

exposing, by plasma (column 9, line 28) deposition reactor, the device to a plasma, the plasma converting the unmasked portions of the conductive layer into a compound (i.e., copper chloride); and

exposing the device to a treatment process, the treatment process selectively removing the compound (column 9, lines 27-58).

Pertaining to claim 32, Allen teaches a method for forming a conductive pattern for a device, comprising:

patterning a mask layer outwardly from a conductive layer of the device, the pattern defining portions of the conductive layer where vias through the conductive layer are desired;

exposing the device to a low energy plasma (please note that the term "low energy" is a relative term), the plasma converting the unmasked portions of the conductive layer into a compound;

and

exposing the device to a treatment process, the treatment process selectively removing the compound.

Conclusion

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

23. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

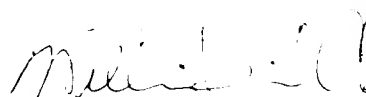
Art Unit: 2823

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 703-305-0004. The examiner can normally be reached on 9:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



W. David Coleman
Examiner
Art Unit 2823

WDC
March 19, 2003